PAGE 2

AX11015 & AX11025 Chip
H/W Configuration Pins
25MHz Crystal
RJ-45 Connector
DoCD HAD Debugger Connector

UART0/1/2 Schematic
UART 0&1: RS-232/9 pin/M
UART 2 : RS-232/9 pin/M
UART 2 : RS-485 FULL/Half
RS232 Transceiver : ZT3243F
RS485 Transceiver : ZT491E

PAGE 8

GPIO Schematic
GPIO 2 : DIP-SW
GPIO 3 : LED Display
Power/GND Connetors

PAGE 3

BUS DIP Switches
Multi-function Pins DIP Switches
GPIO/Timer/INT1/PCA Interfaces
Connectors

PAGE 6

Serial Bus Schematic
I2C : AT24C02A EEPROM
SPI : AT25128 EEPROM (optional)
1-wire : DS18B20 Temperature Sensor
CAN : MAX3050 (for AX11025 only)

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Power and Reset Schematic
Reset Circuit
Input Power : 5V / 1A
Regulator 5V to 3.3 V / 1A

PAGE 4

External Memory Schematic
Flash Memory : 512K * 1
MX29LV004BTC-70
Asy-SRAM : 512K * 2
IC61LV5128-10ns

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Local Bus Schematic
Local Bus Interface Connector
(20*4)

Note: Please refer to AX110xx Network SoC Application Design Note for more detailed information.

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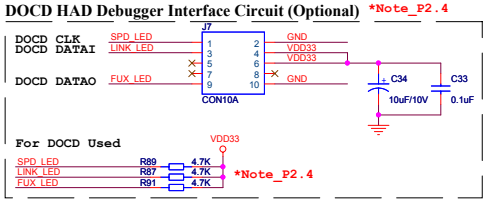
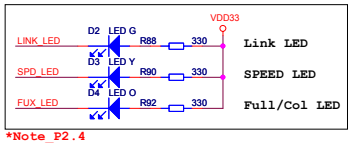
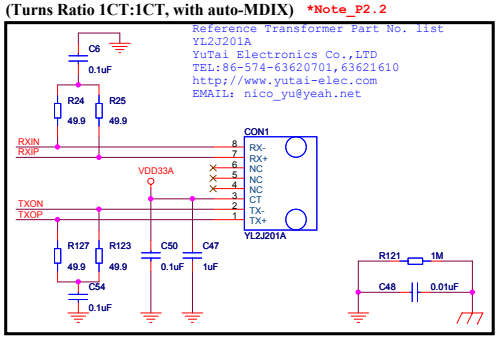
DOCD HAD Debugger Interface Circuit (Optional) *Note_P2.4

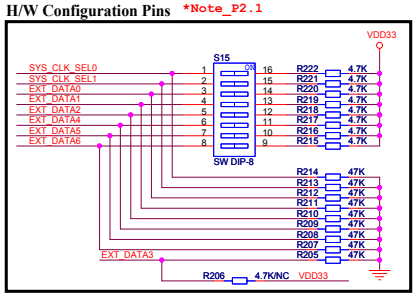




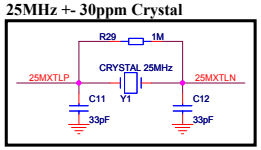
RJ-45 Connector + Tranformer (Turns Ratio 1CT:1CT, with auto-MDIX) *Note_P2.2



H/W Configuration Pins *Note_P2.1



25MHz +- 30ppm Crystal



S15.2-15/S15.1-16
(SYS_CLK_SEL0/SYS_CLK_SEL1)
System CLK Select
00 : 25MHZ 01 : 50MHZ
10 : Don't use 11 : 100MHZ(V)

S15.3-14 (EXT_DATA0)
Ext_Prog_Sram_En
0 : Disable(V) 1 : Enable

S15.4-13 (EXT_DATA1)
Local Bus Mode
0 : Master 1: Slave(V)

S15.5-12 (EXT_DATA2)
Synchronous Bus
0 : Async(V) 1 : Sync

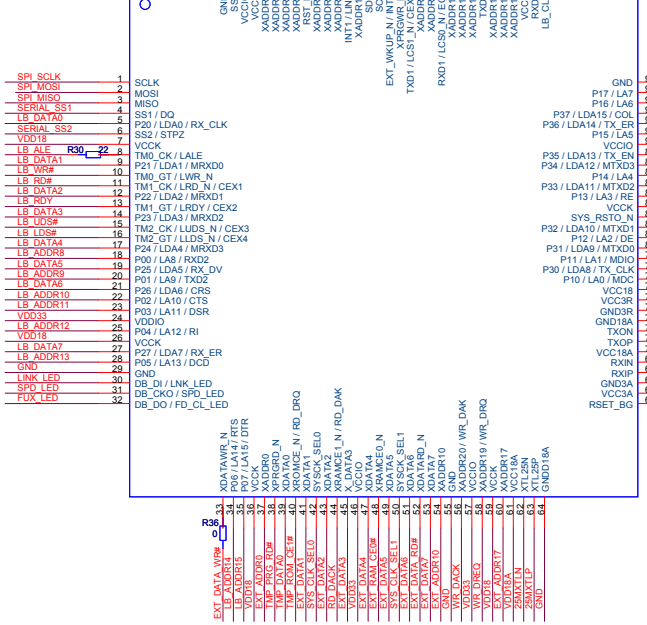
S15.6-11 (EXT_DATA4)(Required)
Burn Flash Enable
0 : Disable(V) 1 : Enable

S15.7-10 (EXT_DATA5)
Burn Flash Baud Rate
0 : 115200(V) 1 : 921K

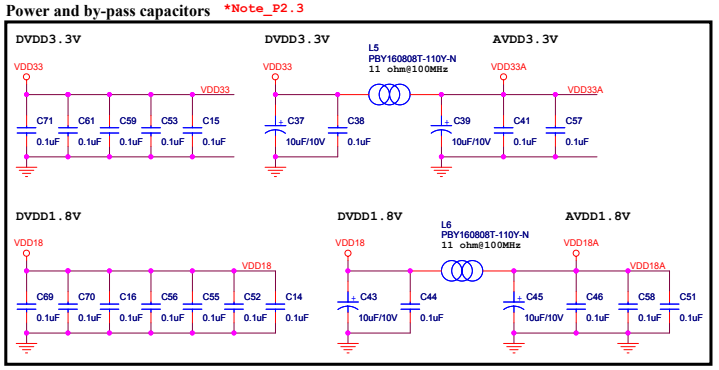
S15.8-9 (EXT_DATA6)(Required)
I2C Boot Disable
0 : Normal(V) 1 : Disable

EXT_DATA3 Test SpeedUp
0 : Normal(V) 1 : Enable

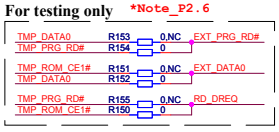
U6 AX11015&AX11025



Power and by-pass capacitors *Note_P2.3



For testing only *Note_P2.6



*Note_P2.3:
All power pins should be implemented with a by-pass capacitor, and the by-pass capacitor should be as close as the power pin. The analog powers and digital powers should be isolated with a Ferrite Bead.

*Note_P2.4:
The DoCD HAD Debugger circuit is optional if you don't need use the DoCD HAD debugger. The DoCD interface pins are shared with the Ethernet LED pins.

*Note_P2.5:
AX110xx on-chip 3.3V to 1.8V regulator is a low dropout regulator (LDO), which requires some large external compensating capacitors on its input (pin #75) and output (pin #76) pins. The C7, C8, C9 and C10 capacitors are the compensating capacitors for the on-chip regulator.

*Note_P2.6:
You can short the (TMP_PRG_RD#, EXT_PRG_RD#), (TMP_DATA0, EXT_DATA0) and (TMP_ROM_CE1#, RD_DREQ) paths directly on your AX110xx schematic. This block circuit is for internal testing purpose only.

*Note_P2.1:
The EXT_DATA4 and EXT_DATA6 configuration pins should be connected to a DIP switch because these two pins need to be configured in the mass production; the other configuration pins can be configured to a default setting based on your requirements. These configuration pins should be pulled high/low through a respective 4.7K/47K resistor and should not be connected to VDD33/GND directly or shared the same resistor each other.

*Note_P2.2:
The TXCT and RXCT pins of magnetic were connected together inside in order to support the Auto-MDIX function. You can select the magnetic without Auto-MDIX function (i.e. the TXCT and RXCT pins are separate) but need to short the TXCT and RXCT pins on your schematic.

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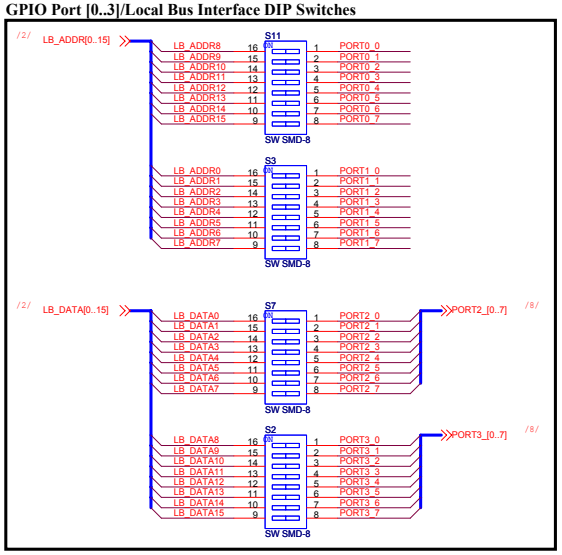
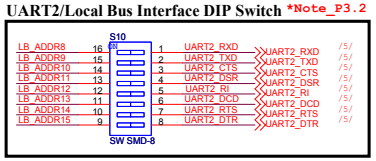
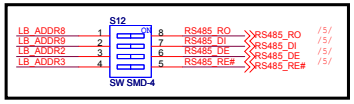
GPIO Port [0..3]/Local Bus Interface DIP Switches



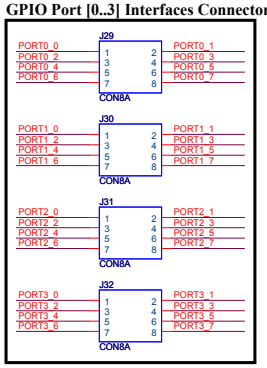
UART2/Local Bus Interface DIP Switch *Note_P3.2



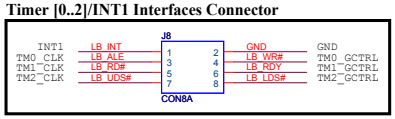
RS-485/Local Bus Interface DIP Switch *Note_P3.2



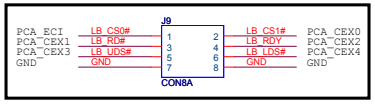
GPIO Port [0..3] Interfaces Connectors

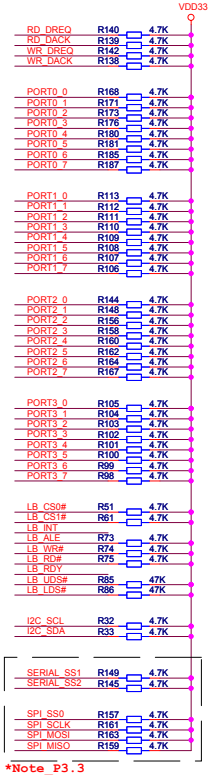


Timer [0..2]/INT1 Interfaces Connector



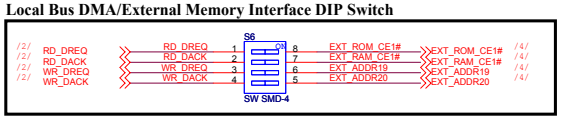
PCA Interface Connector



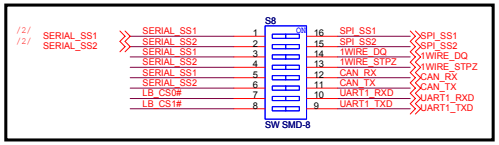


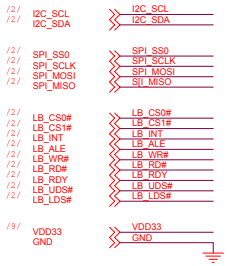
*Note_P3.3

Local Bus DMA/External Memory Interface DIP Switch



SPI/1-Wire/CAN/UART1 Interfaces DIP Switch *Note_P3.1

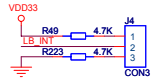


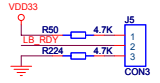


*Note_P3.1:
The (SPI_SS1, SPI_SS2), (1WIRE_DQ, 1WIRE_STPZ) and (CAN_RX, CAN_TX) poles can not be set to ON at the same time because these pins are connected to the SERIAL_SS1 and SERIAL_SS2 pins respectively.

*Note_P3.2:
The UART2 and RS-485 interfaces can not be enabled at the same time since the (UART2_RXD, UART2_TXD) and (RS485_RO, RS485_DI) pins are connected to the same pins (i.e. LB_ADDR8 and LB_ADDR9).

*Note_P3.3:
The AX110xx SPI interface supports 4 types of interface timing mode, namely, Mode 0 ~ Mode 3 by configuring the SPI_CLK and SERIAL_SSx signals. Please refer to Note_P6.5 of page 6 and Section 4.20 of AX11015/AX11025 datasheets for details.





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Title: AX110158&AX11025 EVB - Bus DIP Switches - Setting		
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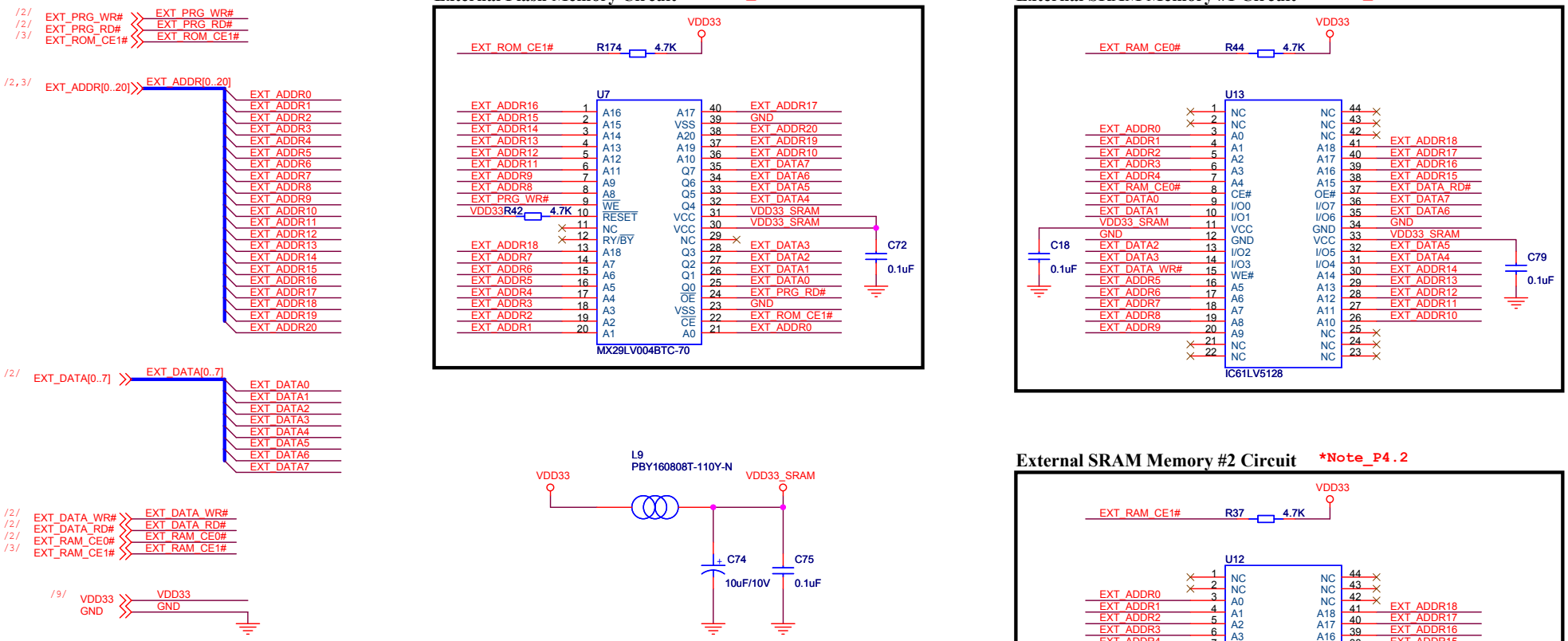

***Note_P4.1:**
The AX11015/AX11025 supports up to 2M bytes external Flash memory.
The external Flash memory is optional for AX110xx applications.

***Note_P4.2:**
The AX11015/AX11025 supports up to 2M bytes external SRAM memory.
The external SRAM memory is optional for AX110xx applications.

ASIX ELECTRONICS CORPORATION		
Title: AX11015&AX11025 EVB - Flash-SRAM		
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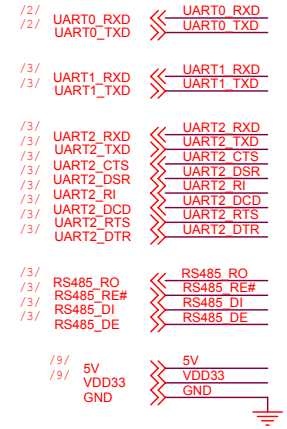
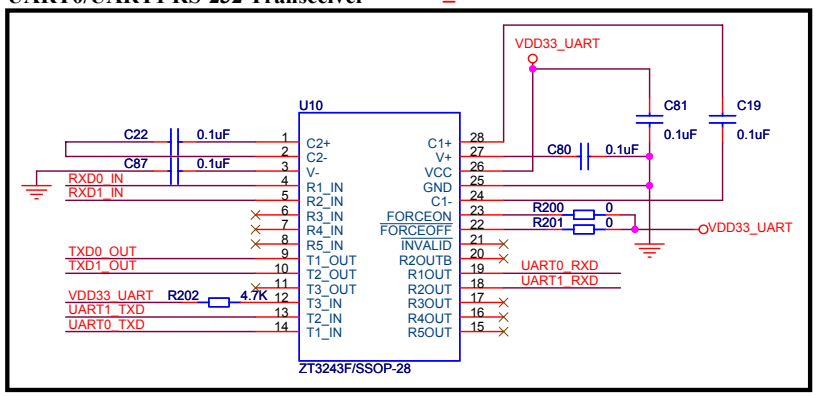
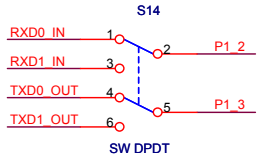


UART0/UART1 RS-232 Transceiver *Note_P5.1

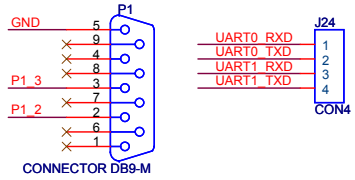


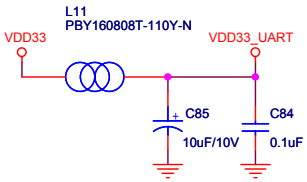
*Note_P5.1

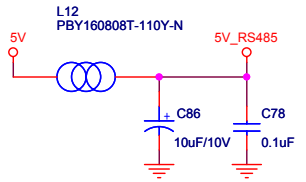
UART0/UART1 Interface Switch



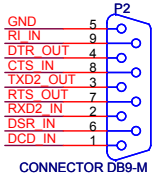
UART0/UART1 RS-232 Connector

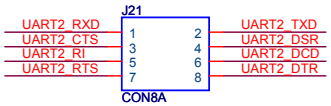




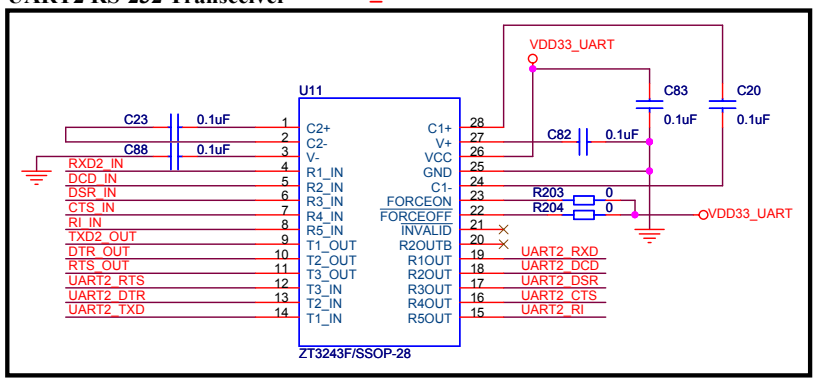


UART2 RS-232 Connector





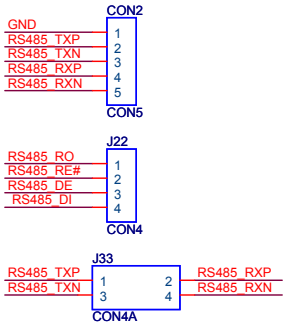
UART2 RS-232 Transceiver *Note_P5.2



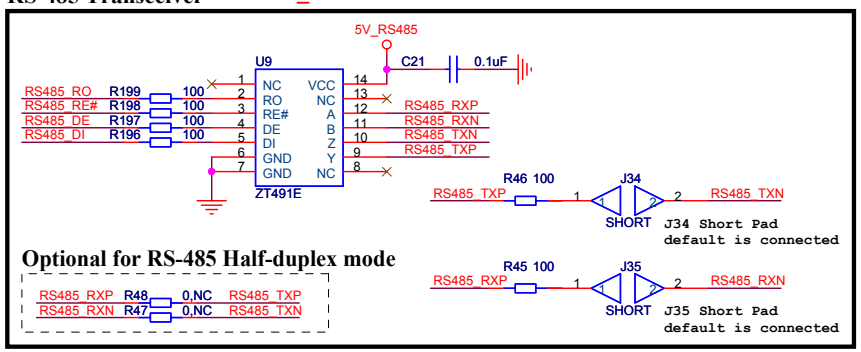
*Note_P5.1:
The UART0 and UART1 interfaces share the same RS-232 port on the AX11015/AX11025 128-pin development boards. You can select the UART0 or UART1 interface by switching the UART0/UART1 interface switch.

*Note_P5.2:
The UART2 and RS-485 interfaces can not be enabled at the same time since the (UART2_RXD, UART2_TXD) and (RS485_RO, RS485_DI) pins are connected to the same pins (i.e. LB_ADDR8 and LB_ADDR9). Please refer to page #3 for more details.

RS-485 Connector



RS-485 Transceiver *Note_P5.2



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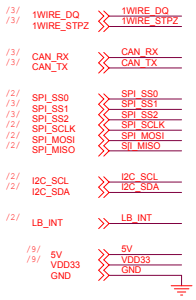
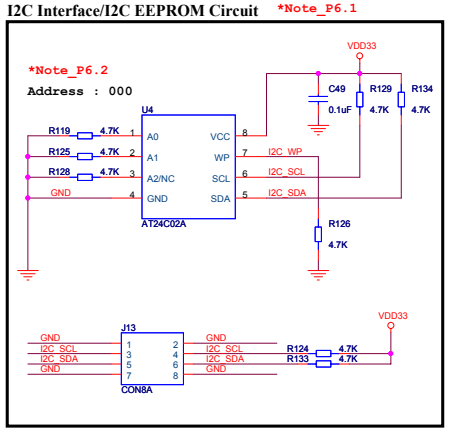
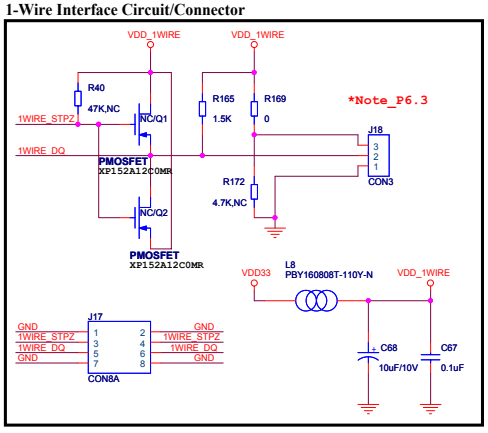


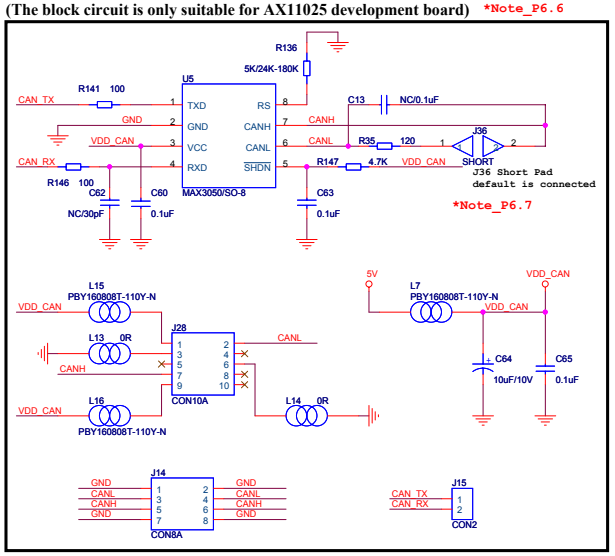
I2C Interface/I2C EEPROM Circuit *Note_P6.1



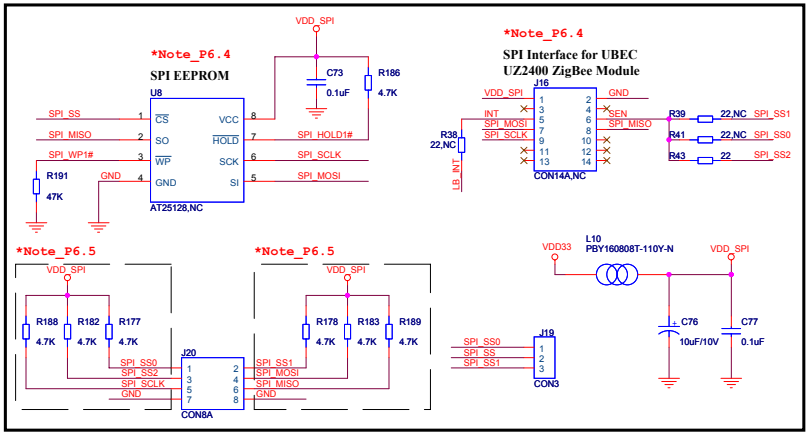
1-Wire Interface Circuit/Connector



CAN Transceiver Interface Circuit
(The block circuit is only suitable for AX11025 development board) *Note_P6.6



SPI Interface Circuit



***Note_P6.1:**
The I2C Configuration EEPROM is used to configure some important AX110xx hardware initialization data and is required for most of AX110xx applications.
AX110xx supports the 24C02~24C16 I2C EEPROM.

***Note_P6.2:**
The 7-bit device address of the I2C Configuration EEPROM should be 1010000b for AX110xx.
That is the A0, A1, A2 signals of the 24C02~24C16 I2C Configuration EEPROM should be pulled down

***Note_P6.3:**
There is a 1-Wire temperature sensor connected to the J18 1-Wire connector on the AX11015 128-pin development board to demonstarte an example of the 1-Wire applications.

***Note_P6.4:**
These are some examples reference circuits of the SPI EEPROM and the SPI interface for the UBEC UZ2400 ZigBee Module.

***Note_P6.5:**
The AX110xx SPI interface supports 4 types of interface timing mode, namely, Mode 0 ~ Mode 3 by configuring the SPI_CLK and SPI_SSx signals.
Please refer to Note_P3.3 pf page 3 and Section 4.20 of AX11015/AX11025 datasheets for details.

***Note_P6.6:**
The CAN interface reference circuit is only suitable for AX11025 applications since the AX11015 doesn't support the CAN interface.

***Note_P6.7:**
Please refer to Appendix A. of AX11025_CAN-to-Ethernet User Guide for more details description of CAN Bus Termination.

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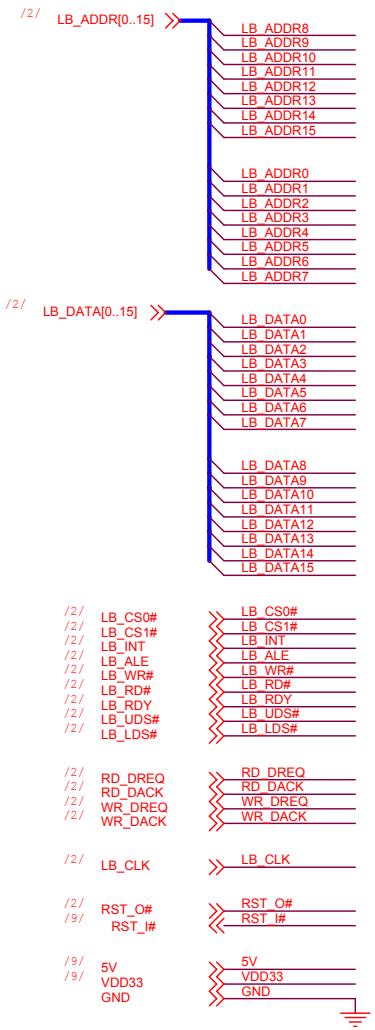
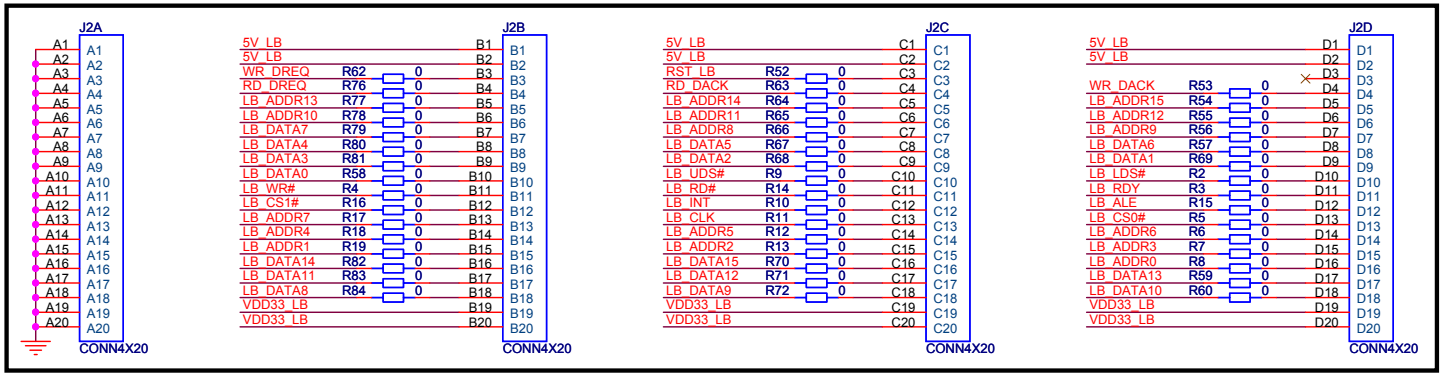
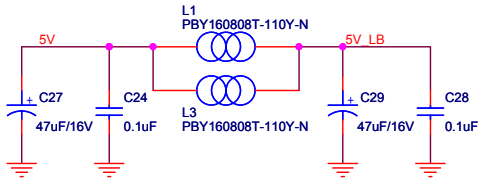
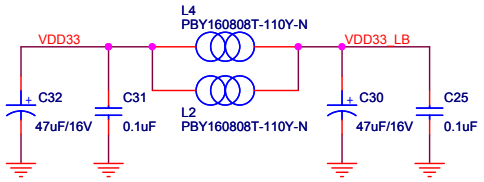
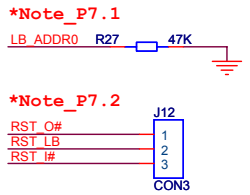


Local Bus Interface Connector









***Note_P7.1:**
The LB_ADDR0 signal should be pulled low when the local bus interface of AX110xx is set to the slave mode and the LB_ADDR0 pin is not used.

***Note_P7.2:**
The RST_O# and RST_LB pins should be short when AX110xx needs to output the reset signal to the external device; the RST_I# and RST_LB pins should be short when the external device needs to reset the AX110xx through the local bus interface.

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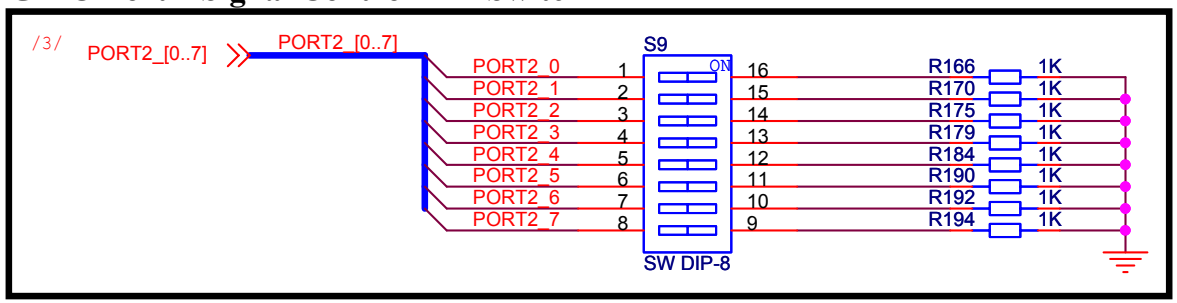
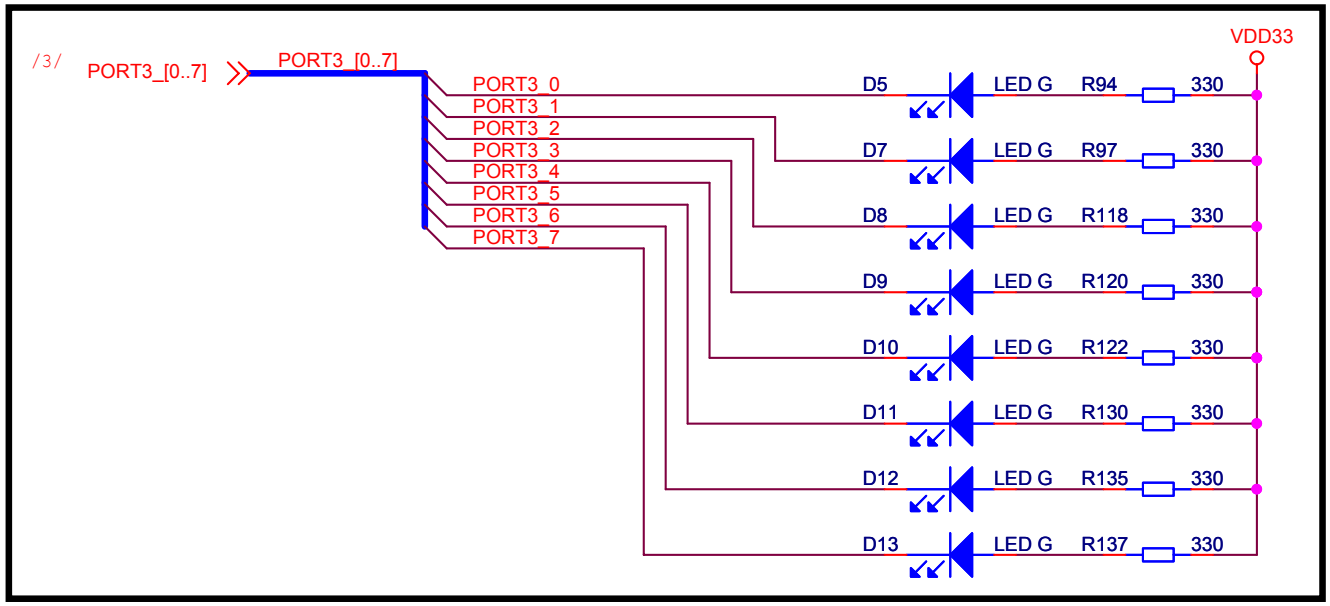
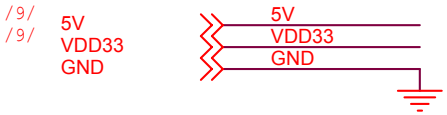
GPIO Port 2 Signal Control DIP Switch

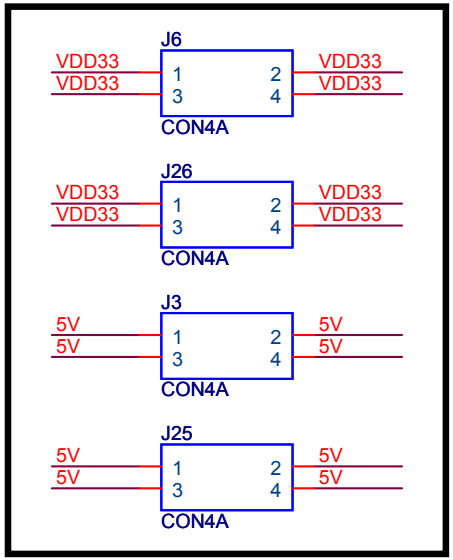


GPIO Port 3 LED Control Circuit *Note_P8.1

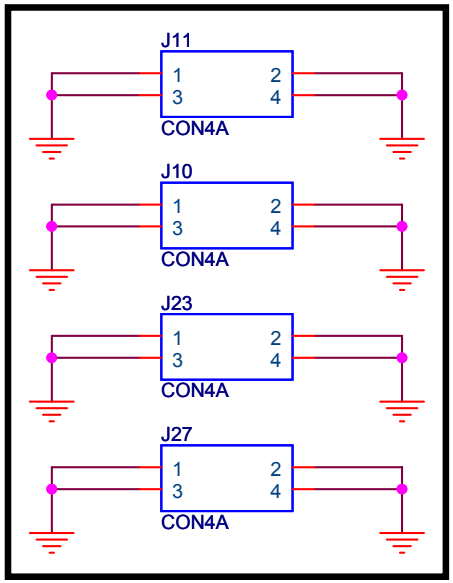




5V/3.3V Power Connectors



GND Connectors



*Note_P8.1:
The GPIO Port 3 LEDs can be controlled by the web server of AX11015/AX11025 demo firmware.

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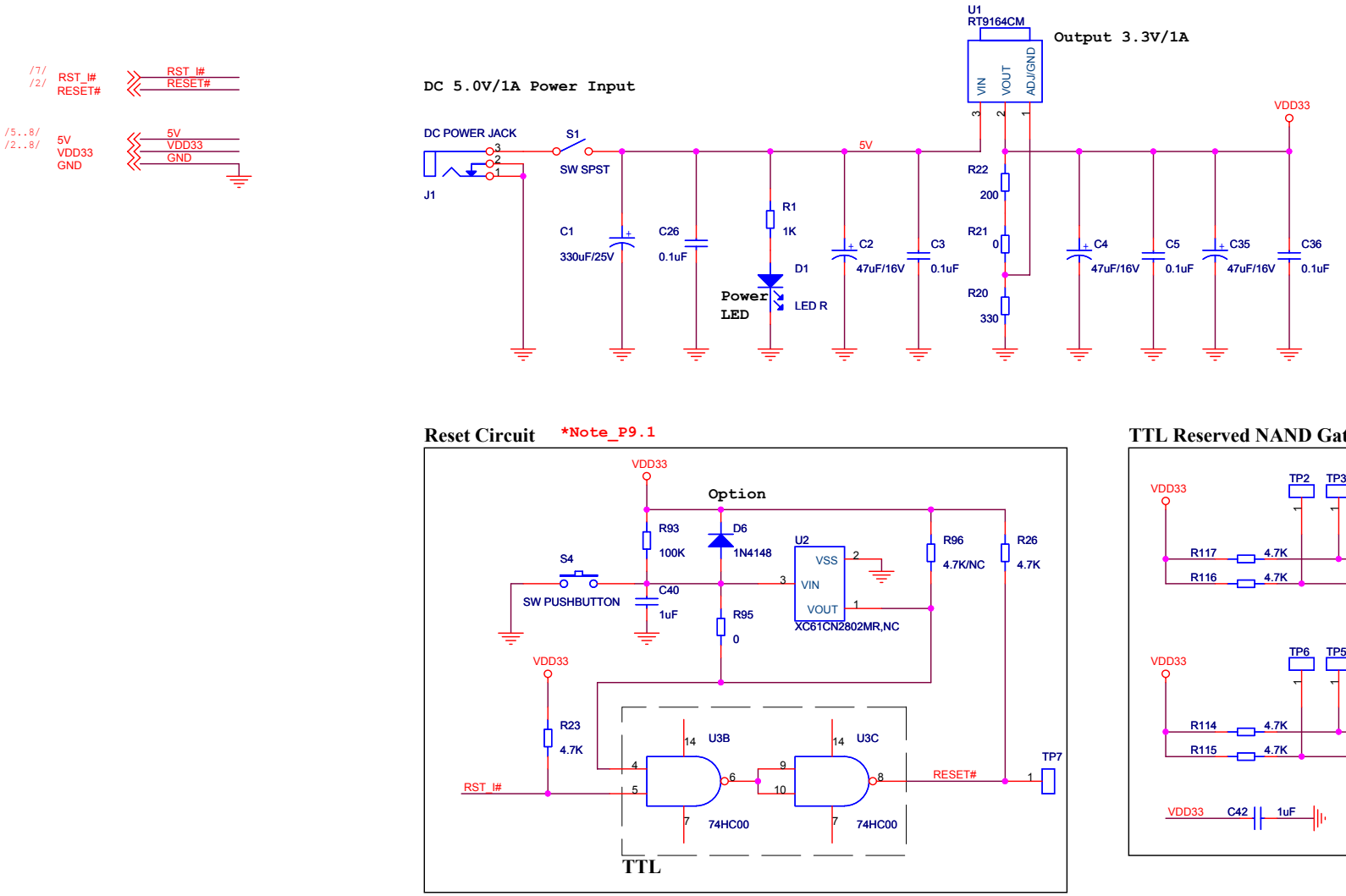

*Note_P9.1:
You can consider using a RC reset circuit on your AX110xx applications if you don't have special requirements.

ASIX ELECTRONICS CORPORATION		
Title: AX11015&AX11025 EVB - Power & Reset		
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V1.00 Init

V1.01
R165 from 4.7K change to 1.5K
R200 and R203 from 0 change to 4.7K,NC
U10 and U11 Pin 23 connect to VDD33_UART

V1.02
R113 from 47K change to 4.7K
R27 from 4.7K change to 47K

V1.20
1. U10.23 connect to VDD33
   U11.23 connect to VDD33
2. Insert Short pad J34 between
   R46.2 and signal RS485_TXN
   Insert Short pad J35 between
   R45.2 and signal RS485_RXN
3. Remove R34
   Insert Short pad J36 between
   R35.2 and signal CANH
4. Increase J28 and L13,L14,L15,L16
   for PCAN to USB
5. C13 0.1uF =>NC
   C62 30pF =>NC
6. R136 value is decided for running
   speed and please reference
   MAXIM MAX3050 datasheet

V1.21
1.The circuit is supported both AX11015&AX11025

V1.22
1.Modify flash describe text for normal and internal test on sheet 2

V1.30 2008/1/17
1. Add some notes to indicate the important information of this schematic.
2. Add the page number information for all off-page symbols.
3. Remove the PORT0_[0..7] and PORT1_[0..7] off-page symbols.
4. Add some notes about the SPI interface timing modes configuration in page 3 and 6.

V1.31 2008/10/28
1. Added more information of the configuration pins circuit in Note_P2.1.

V1.32 2009/10/28
1. Modified the description in Note_P2.1.
2. Added more information of the CAN bus Termination in Note_P6.7
3. Changed default setting to high for Local Bus Mode of H/W Configuration Pins.

ASIX ELECTRONICS CORPORATION		
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