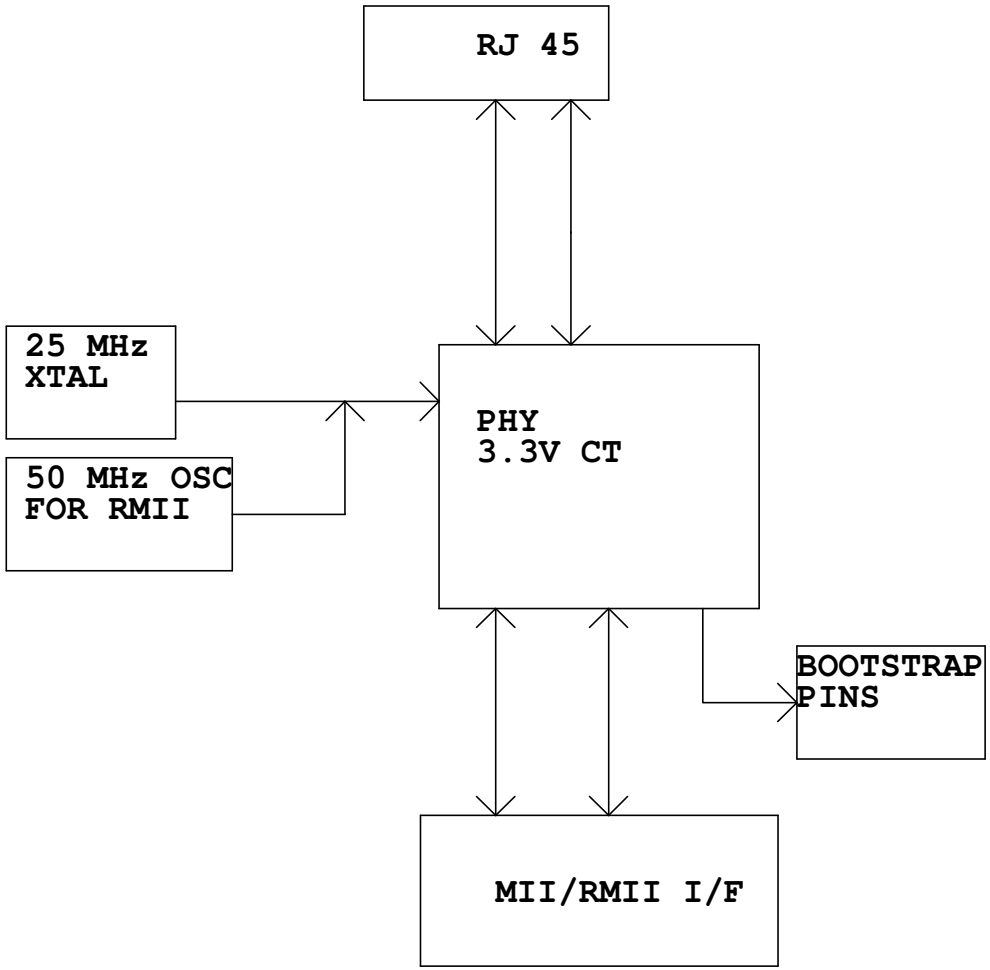
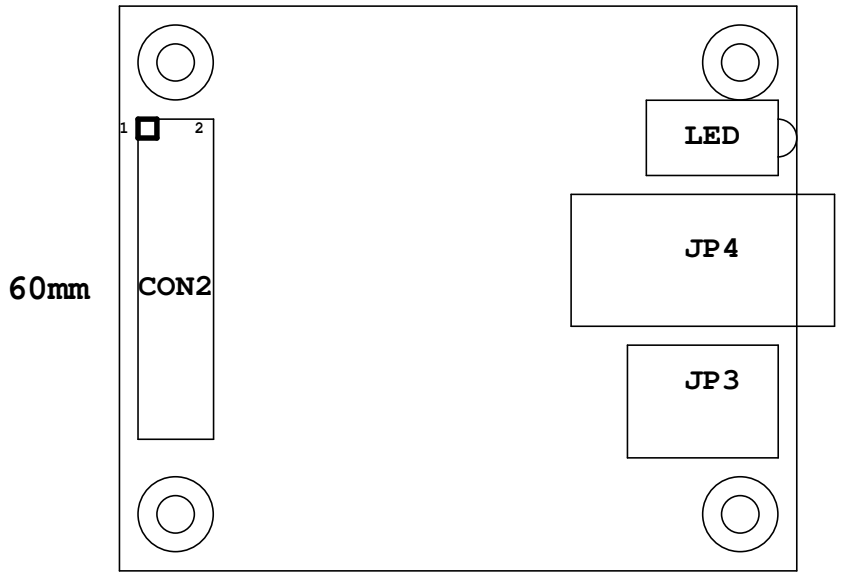
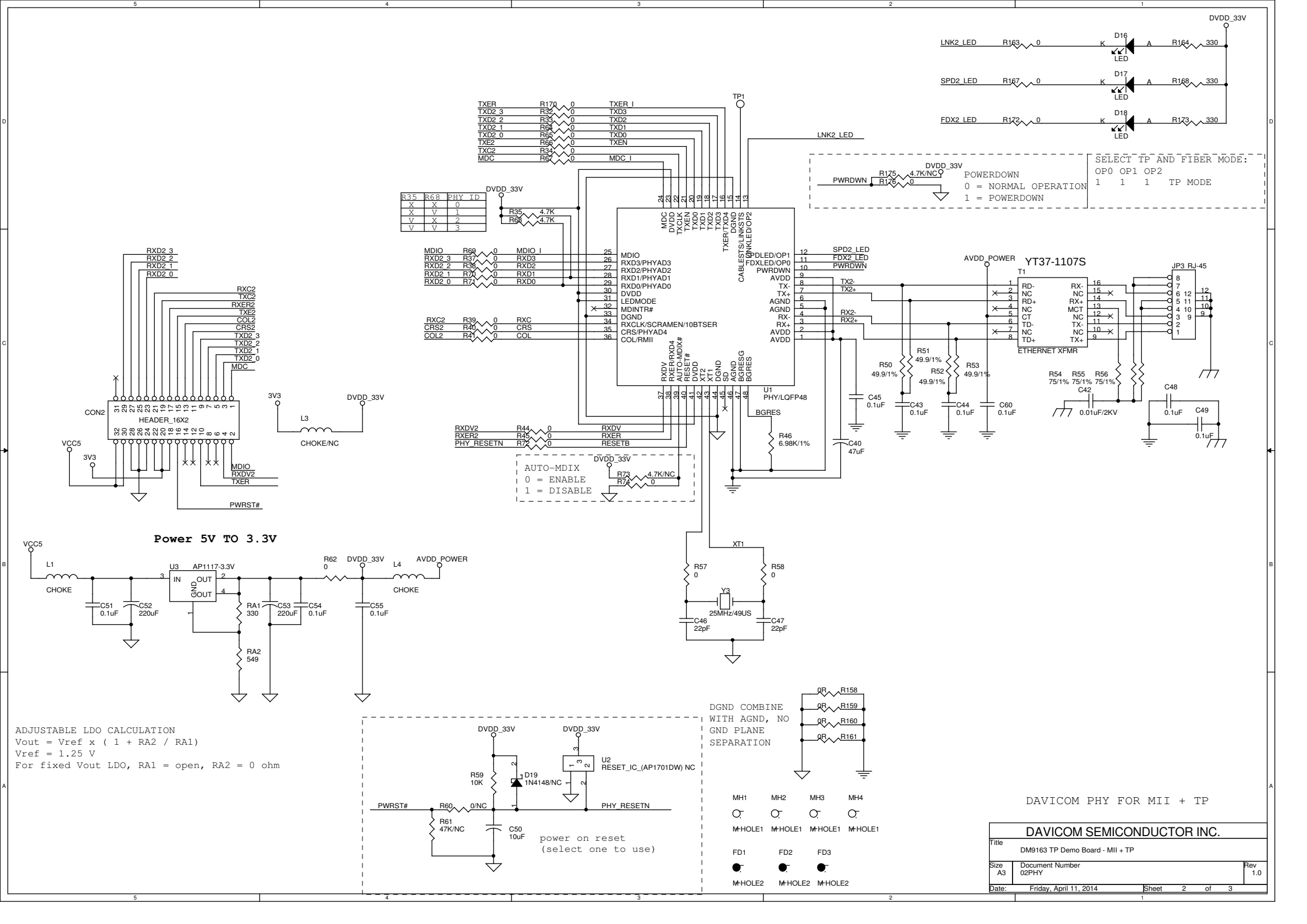
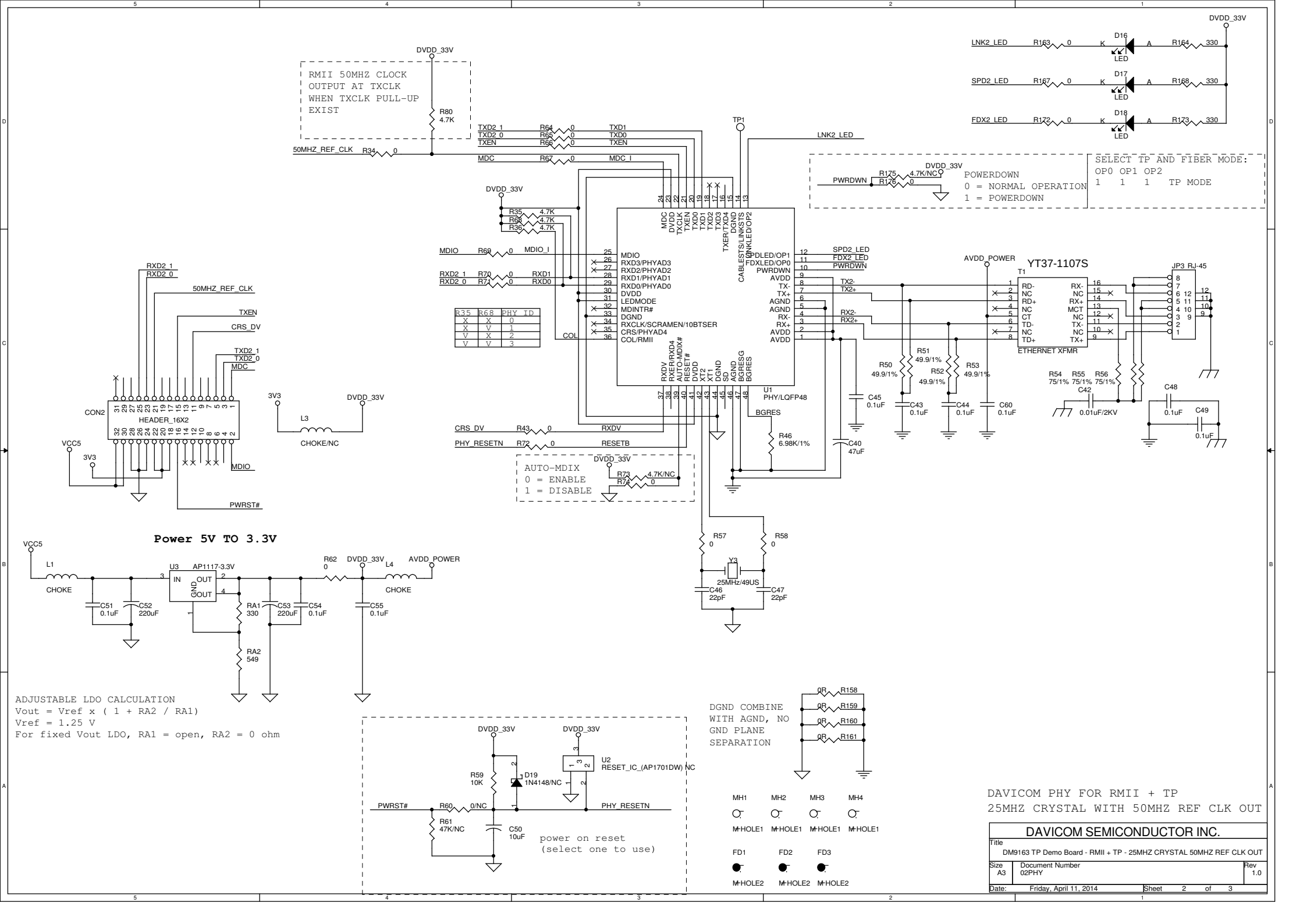


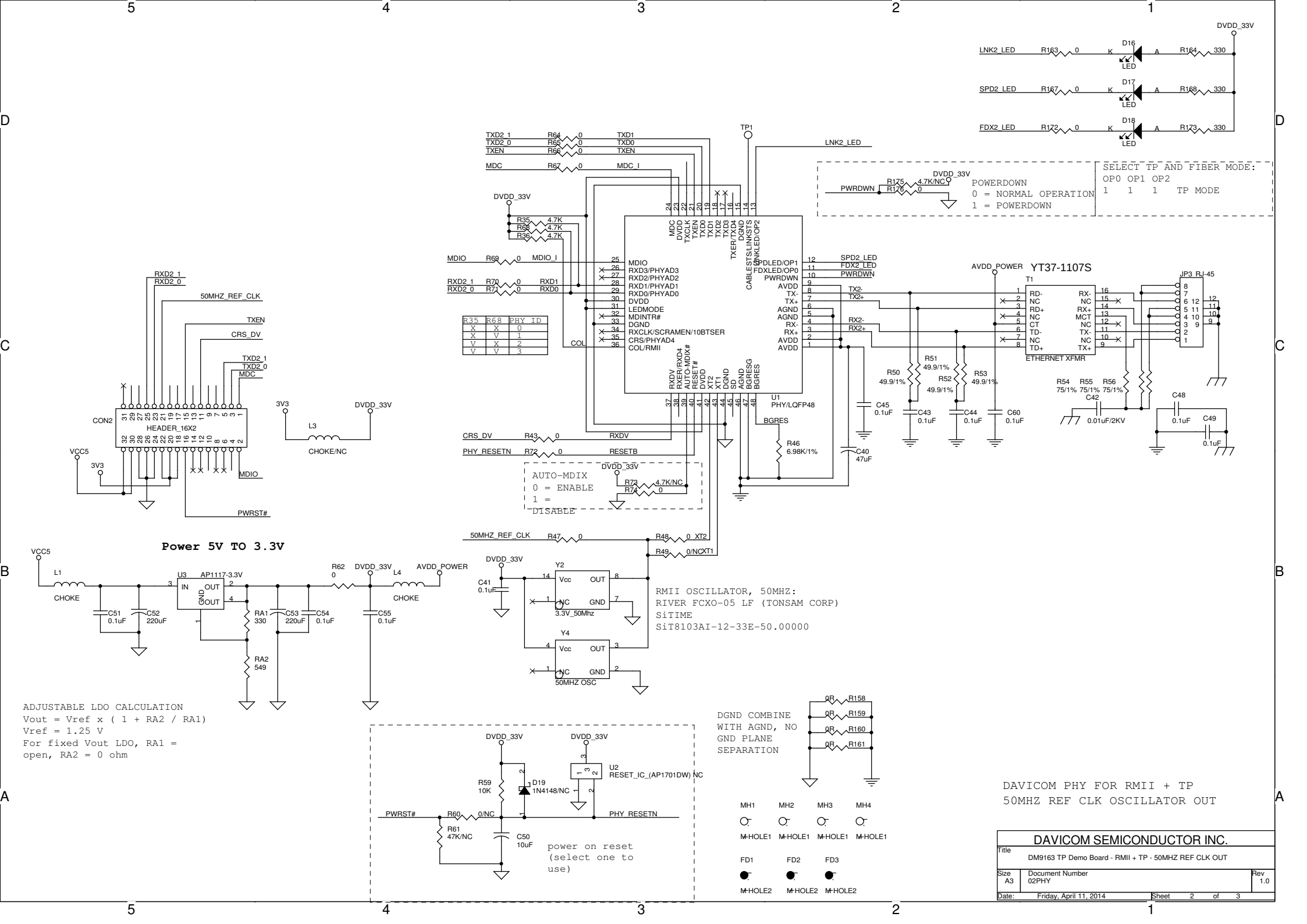


POWER FROM MII
+5V IN
+3.3V OUT
POWER
+3.3V IN
+1.8V OUT

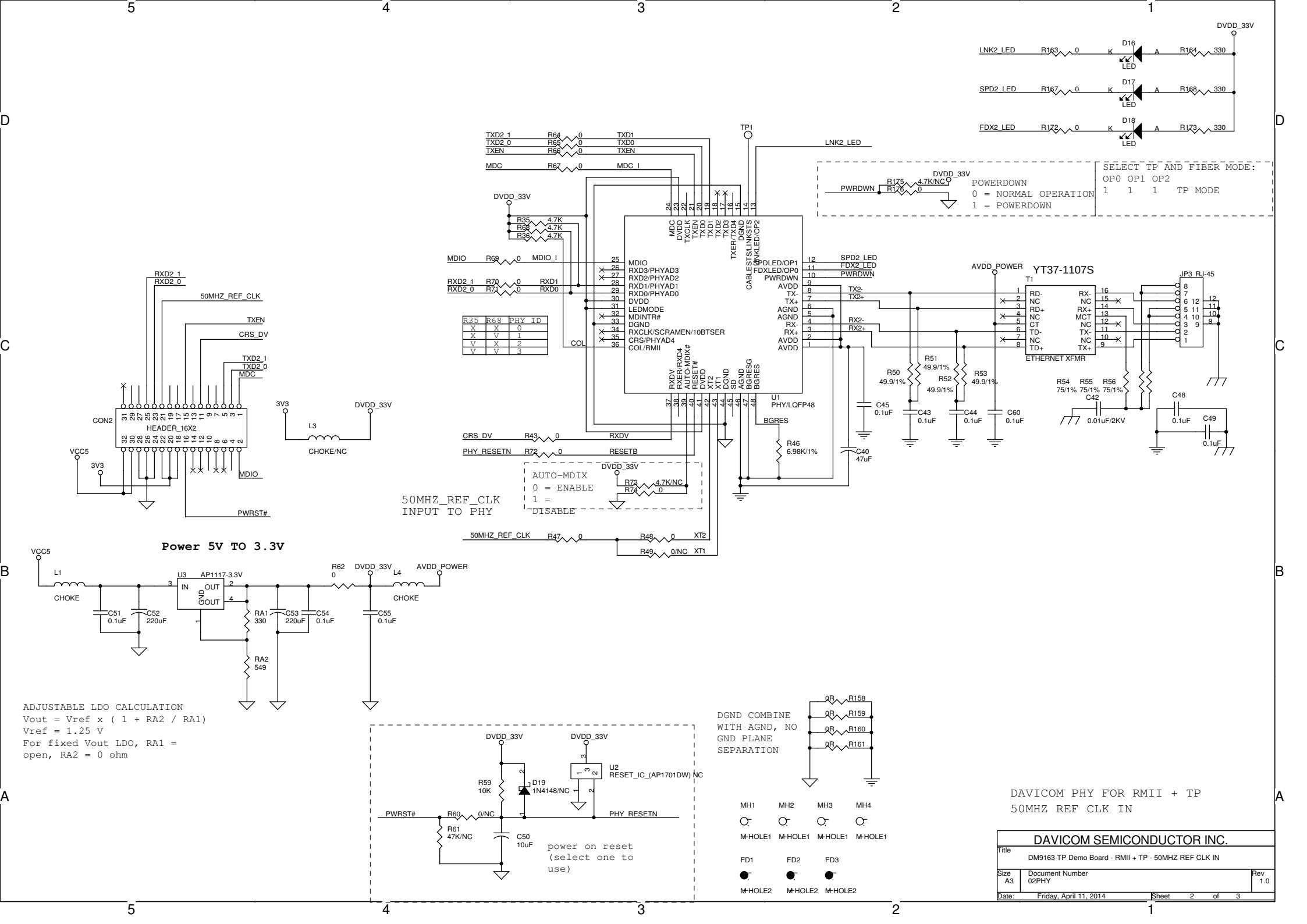
Davicom Semiconductor Inc.		
Title: DM9163 TP Demo Board (PCB_Overview)		
Size: A4	Document Number: 01TOP	Rev: 1.0
Date: Friday, April 11, 2014	Sheet 1 of 3	


DVDD_33V
LNK2_LED R163 0 D16 LED R164 330
SPD2_LED R167 0 D17 LED R168 330
FDX2_LED R172 0 D18 LED R173 330
TP1
TXER R170 0 TXER_I
TXD2_3 R32 0 TXD3
TXD2_2 R33 0 TXD2
TXD2_1 R64 0 TXD1
TXD2_0 R65 0 TXD0
TXE2 R66 0 TXEN
TXC2 R34 0
MDC R67 0 MDC_I
LNK2_LED
PWRDWN R175 4.7K/NC R176 0
POWERDOWN
0 = NORMAL OPERATION
1 = POWERDOWN
SELECT TP AND FIBER MODE:
OP0 OP1 OP2
1 1 1 TP MODE
R35 R68 PHY ID
X X 0
X V 1
V X 2
V V 3
R35 4.7K
R68 4.7K
MDIO R69 0 MDIO_I
RXD2_3 R37 0 RXD3
RXD2_2 R36 0 RXD2
RXD2_1 R70 0 RXD1
RXD2_0 R71 0 RXD0
RXC2 R39 0 RXC
CRS2 R40 0 CRS
COL2 R41 0 COL
MDIO
RXD3/PHYAD3
RXD2/PHYAD2
RXD1/PHYAD1
RXD0/PHYAD0
DVDD
LEDMODE
MDINTR#
DGND
RXCLK/SCRAMEN/10BTSER
CRS/PHYAD4
COL/RMII
SPDLED/OP1
FDXLED/OP0
PWRDWN
AVDD
TX-
TX+
AGND
AGND
RX-
RX+
AVDD
AVDD
U1
PHY/LQFP48
SPD2_LED
FDX2_LED
PWRDWN
TX2-
TX2+
RX2-
RX2+
AVDD_POWER
YT37-1107S
T1
RD-
NC
RD+
NC
CT
TD-
NC
TD+
RX-
NC
RX+
MCT
TX-
NC
TX+
ETHERNET XFMR
JP3 RJ-45
R50 49.9/1%
R51 49.9/1%
R52 49.9/1%
R53 49.9/1%
R54 75/1%
R55 75/1%
R56 75/1%
C42 0.01uF/2KV
C43 0.1uF
C44 0.1uF
C60 0.1uF
C45 0.1uF
C40 47uF
C48 0.1uF
C49 0.1uF
RXD2_3
RXD2_2
RXD2_1
RXD2_0
RXC2
TXC2
RXER2
TXE2
COL2
CRS2
TXD2_3
TXD2_2
TXD2_1
TXD2_0
MDC
CON2
HEADER_16X2
VCC5
3V3
MDIO
RXDV2
TXER
PWRST#
3V3
L3
CHOKE/NC
DVDD_33V
RXDV2 R44 0 RXDV
RXER2 R45 0 RXER
PHY_RESETN R72 0 RESETB
BGRES
R46 6.98K/1%
AUTO-MDIX
0 = ENABLE
1 = DISABLE
R73 4.7K/NC
R74 0
Power 5V TO 3.3V
VCC5
L1
CHOKE
U3 AP1117-3.3V
IN
OUT
GND
OUT
C51 0.1uF
C52 220uF
RA1 330
RA2 549
C53 220uF
C54 0.1uF
R62 0
C55 0.1uF
L4
CHOKE
AVDD_POWER
XT1
R57 0
R58 0
Y3
25MHz/49US
C46 22pF
C47 22pF
ADJUSTABLE LDO CALCULATION
Vout = Vref x (1 + RA2 / RA1)
Vref = 1.25 V
For fixed Vout LDO, RA1 = open, RA2 = 0 ohm
DVDD_33V
DVDD_33V
R59 10K
D19 1N4148/NC
U2 RESET_IC_(AP1701DW) NC
PWRST#
R60 0/NC
PHY_RESETN
R61 47K/NC
C50 10uF
power on reset
(select one to use)
DGND COMBINE WITH AGND, NO GND PLANE SEPARATION
0R R158
0R R159
0R R160
0R R161
MH1 MH2 MH3 MH4
M-HOLE1 M-HOLE1 M-HOLE1 M-HOLE1
FD1 FD2 FD3
M-HOLE2 M-HOLE2 M-HOLE2
DAVICOM PHY FOR MII + TP
DAVICOM SEMICONDUCTOR INC.
Title
DM9163 TP Demo Board - MII + TP
Size A3
Document Number 02PHY
Rev 1.0
Date: Friday, April 11, 2014
Sheet 2 of 3


RMII 50MHZ CLOCK OUTPUT AT TXCLK WHEN TXCLK PULL-UP EXIST
DVDD_33V
R80 4.7K
50MHZ_REF_CLK R34 0
TXD2_1 R64 0 TXD1
TXD2_0 R65 0 TXD0
TXEN R66 0 TXEN
MDC R67 0 MDC_I
MDIO R68 0 MDIO_I
RXD2_1 R70 0 RXD1
RXD2_0 R71 0 RXD0
R35 4.7K
R68 4.7K
R36 4.7K
TP1
LNK2_LED
PWRDWN R175 4.7K/NC R176 0
POWERDOWN
0 = NORMAL OPERATION
1 = POWERDOWN
SELECT TP AND FIBER MODE:
OP0 OP1 OP2
1 1 1 TP MODE
LNK2_LED R163 0 D16 LED R164 330
SPD2_LED R167 0 D17 LED R168 330
FDX2_LED R172 0 D18 LED R173 330
U1 PHY/LQFP48
MDC DVDD TXCLK TXEN TXD0 TXD1 TXD2 TXD3 TXER/TXD4 DGND DKNGS DONKLEDOP2
MDIO RXD3/PHYAD3 RXD2/PHYAD2 RXD1/PHYAD1 RXD0/PHYAD0 DVDD LEDMODE MDINTR# DGND RXCLK/SCRAMEN/10BTSER CRS/PHYAD4 COL/RMII
SPDLED/OP1 FDXLED/OP0 PWRDWN AVDD TX- TX+ AGND AGND RX- RX+ AVDD AVDD
SPD2_LED FDX2_LED PWRDWN
TX2- TX2+ RX2- RX2+
RXDV RXER/RXD4 AUTO-MDIX# RESET# DVDD XT2 XT1 DGND SD AGND BGRESG BGRES
R35 R68 PHY ID
X X 0
X V 1
V X 2
V V 3
COL
CRS_DV R43 0 RXDV
PHY_RESETN R72 0 RESETB
AUTO-MDIX
0 = ENABLE
1 = DISABLE
R73 4.7K/NC R74 0
BGRES R46 6.98K/1%
C45 0.1uF
C40 47uF
AVDD_POWER
T1 YT37-1107S
RD- NC RD+ NC CT TD- NC TD+
RX- NC RX+ MCT NC TX- NC TX+
ETHERNET XFMR
R50 49.9/1%
R51 49.9/1%
R52 49.9/1%
R53 49.9/1%
C43 0.1uF
C44 0.1uF
C60 0.1uF
R54 75/1%
R55 75/1%
R56 75/1%
C42 0.01uF/2KV
C48 0.1uF
C49 0.1uF
JP3 RJ-45
RXD2_1
RXD2_0
50MHZ_REF_CLK
TXEN
CRS_DV
TXD2_1
TXD2_0
MDC
MDIO
PWRST#
CON2 HEADER_16X2
VCC5
3V3
L3 CHOKE/NC
R57 0
R58 0
Y3 25MHz/49US
C46 22pF
C47 22pF
Power 5V TO 3.3V
VCC5
L1 CHOKE
U3 AP1117-3.3V
IN GND OUT OUT
C51 0.1uF
C52 220uF
RA1 330
RA2 549
C53 220uF
C54 0.1uF
R62 0
L4 CHOKE
C55 0.1uF
ADJUSTABLE LDO CALCULATION
Vout = Vref x (1 + RA2 / RA1)
Vref = 1.25 V
For fixed Vout LDO, RA1 = open, RA2 = 0 ohm
DVDD_33V
R59 10K
D19 1N4148/NC
U2 RESET_IC_(AP1701DW) NC
PWRST#
R60 0/NC
PHY_RESETN
R61 47K/NC
C50 10uF
power on reset
(select one to use)
DGND COMBINE WITH AGND, NO GND PLANE SEPARATION
0R R158
0R R159
0R R160
0R R161
MH1 MH2 MH3 MH4
M-HOLE1
FD1 FD2 FD3
M-HOLE2
DAVICOM PHY FOR RMII + TP
25MHZ CRYSTAL WITH 50MHZ REF CLK OUT
DAVICOM SEMICONDUCTOR INC.
Title
DM9163 TP Demo Board - RMII + TP - 25MHZ CRYSTAL 50MHZ REF CLK OUT
Size A3
Document Number 02PHY
Rev 1.0
Date: Friday, April 11, 2014
Sheet 2 of 3



DAVICOM SEMICONDUCTOR INC.	
Title	DM9163 TP Demo Board - RMII + TP - 50MHZ REF CLK OUT
Size A3	Document Number 02PHY
Rev	1.0
Date: Friday, April 11, 2014	Sheet 2 of 3


DVDD_33V
LNK2_LED
SPD2_LED
FDX2_LED
D16
D17
D18
LED
R163 0
R164 330
R167 0
R168 330
R172 0
R173 330
TP1
TXD2_1
TXD2_0
TXEN
MDC
R64 0
R65 0
R66 0
R67 0
TXD1
TXD0
TXEN
MDC_I
R35 4.7K
R64 4.7K
R36 4.7K
MDIO
R69 0
MDIO_I
RXD2_1
RXD2_0
R70 0
R71 0
RXD1
RXD0
COL
MDIO
RXD3/PHYAD3
RXD2/PHYAD2
RXD1/PHYAD1
RXD0/PHYAD0
DVDD
LEDMODE
MDINTR#
DGND
RXCLK/SCRAMEN/10BTSER
CRS/PHYAD4
COL/RMII
RXDV
RXER/RXD4
AUTO-MDIX#
RESET#
DVDD
XT2
XT1
DGND
AGND
AGRESG
BGRES
U1
PHY/LQFP48
SPDLED/OP1
FDXLED/OP0
PWRDWN
AVDD
TX-
TX+
AGND
AGND
RX-
RX+
AVDD
AVDD
SPD2_LED
FDX2_LED
PWRDWN
TX2-
TX2+
RX2-
RX2+
CABLESTS/LINKSTS
DPXLED/OP2
TXER/TXD4
DCRS
R35 R68 PHY ID
X X 0
X V 1
V X 2
V V 3
CRS_DV
R43 0
RXDV
PHY_RESETN
R72 0
RESETB
BGRES
R46 6.98K/1%
C40 47uF
C45 0.1uF
AUTO-MDIX
0 = ENABLE
1 = DISABLE
R73 4.7K/NC
R74 0
50MHZ_REF_CLK
INPUT TO PHY
50MHZ_REF_CLK
R47 0
R48 0
R49 0/NC
XT2
XT1
PWRDWN
R175 4.7K/NC
R176 0
POWERDOWN
0 = NORMAL OPERATION
1 = POWERDOWN
SELECT TP AND FIBER MODE:
OP0 OP1 OP2
1 1 1 TP MODE
AVDD_POWER
YT37-1107S
T1
RD-
NC
RD+
NC
CT
TD-
NC
TD+
RX-
NC
RX+
MCT
NC
TX-
NC
TX+
ETHERNET XFMR
JP3 RJ-45
R50 49.9/1%
R51 49.9/1%
R52 49.9/1%
R53 49.9/1%
C43 0.1uF
C44 0.1uF
C60 0.1uF
R54 75/1%
R55 75/1%
R56 75/1%
C42 0.01uF/2KV
C48 0.1uF
C49 0.1uF
RXD2_1
RXD2_0
50MHZ_REF_CLK
TXEN
CRS_DV
TXD2_1
TXD2_0
MDC
MDIO
PWRST#
CON2
HEADER_16X2
VCC5
3V3
3V3
L3
CHOKE/NC
DVDD_33V
Power 5V TO 3.3V
VCC5
L1
CHOKE
U3
AP1117-3.3V
IN
OUT
GND
OUT
C51 0.1uF
C52 220uF
RA1 330
RA2 549
C53 220uF
C54 0.1uF
R62 0
DVDD_33V
L4
CHOKE
AVDD_POWER
C55 0.1uF
ADJUSTABLE LDO CALCULATION
Vout = Vref x (1 + RA2 / RA1)
Vref = 1.25 V
For fixed Vout LDO, RA1 =
open, RA2 = 0 ohm
DVDD_33V
DVDD_33V
R59 10K
D19 1N4148/NC
U2
RESET_IC_(AP1701DW) NC
PWRST#
R60 0/NC
PHY_RESETN
R61 47K/NC
C50 10uF
power on reset
(select one to
use)
DGND COMBINE
WITH AGND, NO
GND PLANE
SEPARATION
0R R158
0R R159
0R R160
0R R161
MH1
MH2
MH3
MH4
M-HOLE1
FD1
FD2
FD3
M-HOLE2
DAVICOM PHY FOR RMII + TP
50MHZ REF CLK IN
DAVICOM SEMICONDUCTOR INC.
Title
DM9163 TP Demo Board - RMII + TP - 50MHZ REF CLK IN
Size
A3
Document Number
02PHY
Rev
1.0
Date:
Friday, April 11, 2014
Sheet
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of
3

VER	DATE	ENGINEER	NOTE
1.0	04/10/2014	WILLIE NIOU	INITAL CIRCUIT CREATION

Davicom Semiconductor Inc.		
Title: DM9163 TP Demo Board (History)		
Size: A4	Document Number: HISTORY	Rev: 1.0
Date: Friday, April 11, 2014	Sheet 3 of 3	